SiGe-on-insulator prepared by wafer bonding and layer transfer for high-performance field-effect transistors

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L. J. Huang,[a] J. O. Chu, D. F. Canaperi, C. P. D'Emic, R. M. Anderson, S. J. Koester, and H.-S. Philip Wong
IBM T. J. Watson Research Center, Yorktown Heights, New York 10598

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SiGe-on-insulator material was fabricated by wafer bonding and hydrogen-induced layer transfer techniques. The transferred SiGe layer is strain relaxed and has a Ge content ranging from 15% to 25%. High-quality strained Si layers were grown on the SiGe-on-insulator substrates by the UHV/chemical vapor deposition process at 550 °C. An electron mobility of 40 000 $cm^2/V\,s$ in a modulation-doped Si/SiGe heterostructure was achieved at 30 K on a SiGe-on-insulator substrate.
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Enhanced electron and hole mobility in strained Si and SiGe has been previously reported. In modulation-doped field-effect-transistors (MODFETs), electron and hole mobilities in Si under tensile strain and SiGe under compressive strain are 2200–2800 and 800–1050 $cm^2/V\,s$, respectively, exceeding the electron and hole mobilities in bulk Si by 3–5 times.[1,2] For the complementary metal–oxide–semiconductor (CMOS) very large scale integration (VLSI) applications, mobility enhancement of electrons and holes by 60%–80% was also reported in strained Si in metal–oxide–semiconductor field-effect transistors (MOSFETs).[3,4] The use of the strained Si/SiGe material system to replace bulk Si in state-of-the-art VLSI technologies is very promising to provide high performance CMOS in the sub-100 nm regime. Most recently, the merging of strained Si/SiGe and silicon-on-insulator technologies has attracted increasing interest because of its great potential to realize high performance MODFET and MOSFET.[5,6]

The ability to prepare high-quality SiGe-on-insulator (SGOI) material is critical for the practical application of the SGOI technology. Strained Si MOSFET devices with enhanced performance have been demonstrated in SGOI material fabricated by separation-by-implanted-oxygen technology for n-type and p-type devices.[6] However, the oxygen implantation and high annealing temperature (>1300 °C) used raise concerns regarding the quality of the relaxed SiGe buffer on which the strained Si channel is grown, especially when the Ge concentration needs to be higher than 10%. In this report, we describe a method of preparing high-quality SGOI material through wafer bonding and H-induced layer transfer techniques. Device-quality strained Si layers have been grown epitaxially on the SGOI substrates and very high electron mobility has been demonstrated in a modulation-doped layer structure.

Strain-relaxed SiGe layers with uniform Ge content in the range of 15%–30% were grown on 5 in. p-type Si substrates by the UHV/chemical vapor deposition (CVD) method in the temperature range of 500–550 °C.[7] The total SiGe epilayer thickness is in the range of 1–2 μm. The degree of relaxation of the strain-relaxed SiGe layers was determined by x-ray diffraction measurements[8] to be >90%. The Si substrates with the relaxed SiGe epilayers were implanted by hydrogen (H_2^+) with a dose of 2.5–5.0 $\times 10^{16}/cm^2$, which is typical for the Smart-Cut® process.[9] The implantation energy was chosen based on TRIM simulations so that the hydrogen peak (R_p) is located in the top portion of the relaxed SiGe layer and is well above the network of misfit dislocations at the epigrowth interface that relieve the lattice mismatch strain. A blistering study was used to determine the optimal implantation and thermal annealing conditions for the SiGe layer transfer process.

The H-implanted substrates were then polished by a chemical-mechanical planarization (CMP) process and cleaned by highly concentrated dissolved ozone in water followed by a diluted Radio Corporation of America clean.[10] A room temperature bonding process was used to bond each H-implanted SiGe/Si substrate to a second 5 in. Si handle wafer that had 300 nm thermally grown SiO_2. During the subsequent thermal treatment in the temperature range of 300–550 °C, layer splitting took place in the SiGe layer where the H-induced microcracks formed. The H-induced splitting in the relaxed SiGe layer resulted in the transferring of a ~500 nm relaxed SiGe layer onto the second handle substrate thereby forming of a SGOI substrate. The described process for achieving strained Si on SGOI substrate is schematically shown in Fig. 1. The layer quality of SiGe is investigated by transmission electron microscope (TEM). For device fabrication, a simple strained Si channel layer or in combination with a modulation-doped layered structure can be grown on the SGOI substrate after further smoothing and cleaning of the as-split SGOI substrate. In this work, a simple modulation-doped multilayer structure was grown on the SGOI substrates to study the electron transport characteristics in the strained Si layer.

We first studied the H-induced surface blistering in a relaxed $Si_{1-x}Ge_x$ (x=15%–30%) layer epitaxially grown on a Si substrate. Using a blistering study[11] in the unbonded SiGe/Si substrates provides us a simple way to study the feasibility of H-induced layer splitting in a relaxed SiGe layer and to determine the optimal hydrogen implantation conditions. Figure 2 shows the cross-sectional TEM of a $Si_{0.85}Ge_{0.15}$ layer implanted by hydrogen at 120 keV with a

[a]Electronic mail: ljhuang@us.ibm.com

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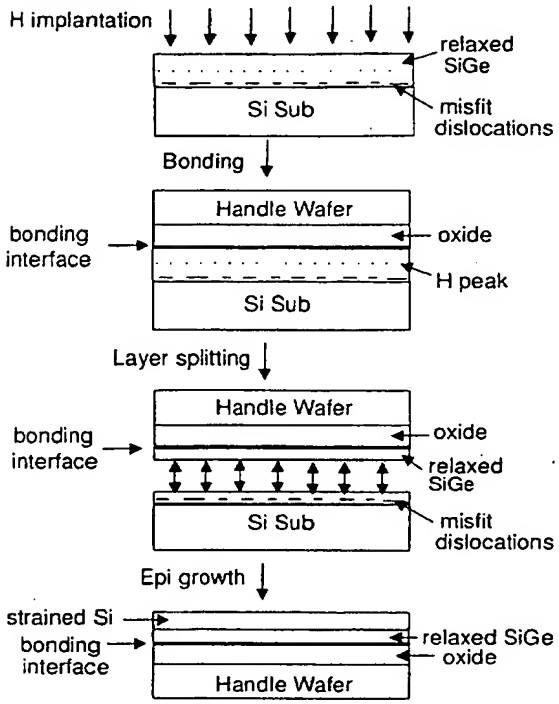

FIG. 1. Process flow for making strained Si on SiGe-on-insulator material by wafer bonding and H-induced layer transfer.

H_2^+ dose of $3.5\times10^{16}/cm^2$. The sample was subsequently annealed in N_2 at 500 °C for 1 h. Microcracks with a size up to 100 nm were observed in the high H concentration region. It can also be seen that some microcracks were decorated with microvoids, which may be associated with the formation of H_2 molecules in vacancy clusters agglomerated during the thermal annealing. The observed uniform surface blistering on the sample, as shown in Fig. 3, suggests possible layer splitting in the relaxed SiGe layer if it is bonded to a second substrate.

By applying wafer bonding to H-implanted SiGe substrates, we have demonstrated layer transfer of SiGe layers with Ge content up to 25% across 5 in. substrates onto handle substrates with an insulating SiO_2 layer thereby creating the SGOI material structure. The SiGe epilayers were smoothed with a CMP process prior to room temperature wafer bonding. The CMP process developed in this work allows us to reduce the surface roughness of SiGe from 8–10 nm rms to ~0.5 nm rms while keeping the layer thickness variation across the 5 in. wafers to be less than 10%. The bonded SiGe-to-oxide wafers were then annealed at 500–600 °C to induce layer splitting in SiGe. The SGOI substrates with the transferred SiGe layers were annealed at 800–900 °C to strengthen the bonding interface. A high-resolution cross-section TEM image of the SGOI substrate is shown in Fig. 4, which reveals no threading dislocations in the transferred SiGe layer. Planar view TEM estimated the threading dislocation density in the transferred SiGe layer to be $\sim10^6/cm^2$. Furthermore, since only the top-most portion of the SiGe layer is transferred to the handle wafer, the misfit dislocations associated with the lattice mismatch at the Si/SiGe growth interface are eliminated. Consequently, the amount of defects in the final SiGe-on-insulator substrate is significantly reduced in comparison to the original SiGe/Si seed substrate. It is worth mentioning here that SiGe layers with 30% Ge were also bonded and split. However, the transferred $Si_{0.7}Ge_{0.3}$ layers appeared to be hazy with a large number of "islands" on the surface. The poor quality of the transferred SiGe with higher Ge content might be due to agglomeration or precipitation of Ge during the bonding or the splitting annealing step. Low-temperature bonding and splitting processes are desirable to make SGOI material with a wider range of Ge concentrations for its potential applica-

FIG. 2. Cross-section TEM of H-implanted $Si_{0.85}Ge_{0.15}$ (implantation: H_2^+, 120 keV, $3.5\times10^{16}/cm^2$; annealed at 550 °C, 1 h).

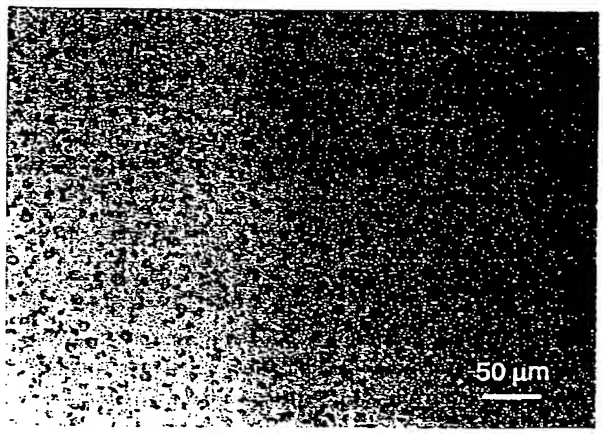

FIG. 3. Surface blistering in H-implanted $Si_{0.85}Ge_{0.15}$ observed by optical microscope (implantation: H_2^+, 120 keV, $3.5\times10^{16}/cm^2$; annealed at 550 °C, 1 h).

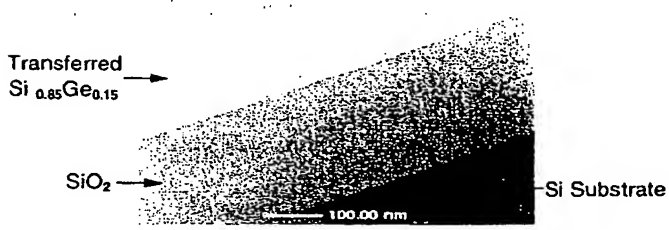

FIG. 4. Cross-section TEM of a SGOI substrate prepared by wafer bonding and H-induced layer transfer.

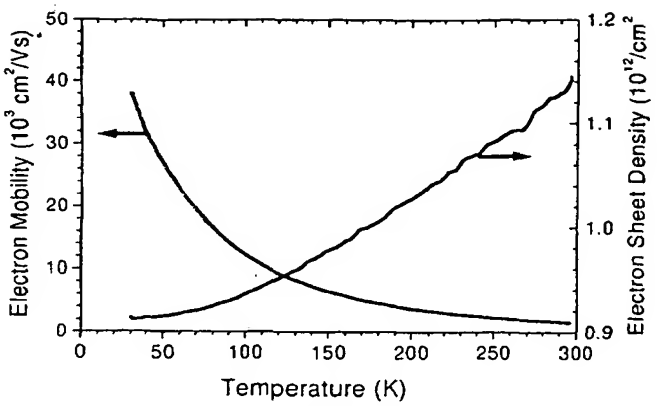

FIG. 5. Electron density and mobility as a function of temperature in a modulation-doped structure grown on a SGOI substrate (Ge content is 20%).

tions in high speed electronic or optical devices.

The as-split SGOI substrate has a surface roughness of 6–8 nm rms, therefore a CMP process step is needed to smooth the surface of the transferred SiGe layer prior to the epitaxial growth of strained Si or any other SiGe device structures. While improving the surface roughness to ~0.5 nm rms, the thickness of the transferred SiGe layer can also be tailored via CMP for different applications, e.g., <100 nm SiGe layer is required for state-of-the-art VLSI CMOS technology.

To investigate the feasibility of device application of the SGOI material, we have grown a simple modulation-doped multilayer structure on a SGOI substrate to study the carrier transport behavior in the tensile-strained Si channel. By excluding such device fabrication requirements as source/drain implantation and dopant activation annealing, etc., the modulation-doped structure provides us with an easy device structure to study the quality of the transferred SiGe layer and the overgrown strained Si channel. The modulation-doped Si/SiGe multilayer structure, consisting of (from top to bottom) Si cap layer, n^+ SiGe supply layer, intrinsic SiGe spacer, intrinsic strained Si channel, and ~100 nm $Si_{0.8}Ge_{0.2}$ extended buffer layer, was grown via UHV/CVD on 5 in. SGOI substrates with starting transferred $Si_{0.8}Ge_{0.2}$ layer of about 300 nm. Ag/Sb was used for metallization.

Temperature dependent Hall measurements were used to determine the electron carrier density and mobility in the strained Si channel in the SiGe heterostructure described earlier. Figure 5 shows the measured electron density and mobility as a function of temperature. It can be seen that the electron density decreases as the sample is cooled down below room temperature, suggesting freeze-out of the carriers in the n^+-doped SiGe supply layer. However, at temperatures below 75 K, the electron density plateaus at a level of 9.0×10^{11}/cm^2, which is an indication of the confinement of a two-dimensional electron gas in a quantum well as defined by the band gap offset in the strained Si channel and the relaxed SiGe buffer layer. The electron mobility increases to ~40 000 cm^2/V s at temperatures below 30 K, which is comparable to the electron mobility measured in a similar device structure grown on a bulk Si substrate.[12] The electrical results shown in Fig. 5 indicate the high quality of the strained Si channel achieved on the SGOI substrate, demonstrating the feasibility of fabricating high-speed FET devices in a strained Si layer on a SGOI substrate.

In summary, we have demonstrated SiGe-on-insulator material using wafer bonding and hydrogen-induced layer transferring techniques. Two-dimensional electron gas behavior and very high electron mobility in a strained Si layer has been demonstrated in a modulation-doped structure grown on the SGOI substrates. Device-quality strained Si on 5 in. SGOI substrates with different Ge composition has been fabricated and is currently being used for making high-speed MOSFET devices.

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